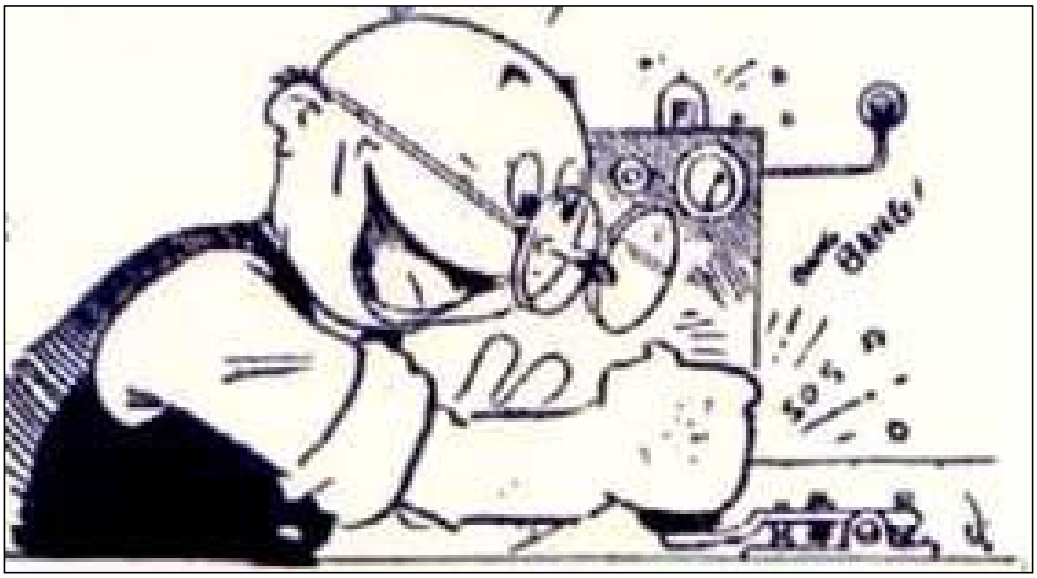
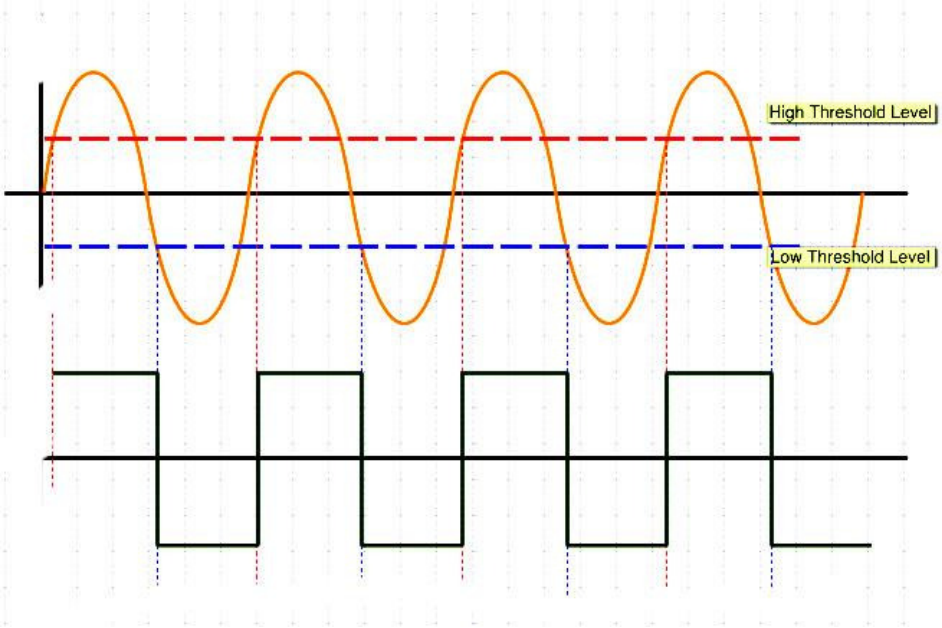
Who's counting?



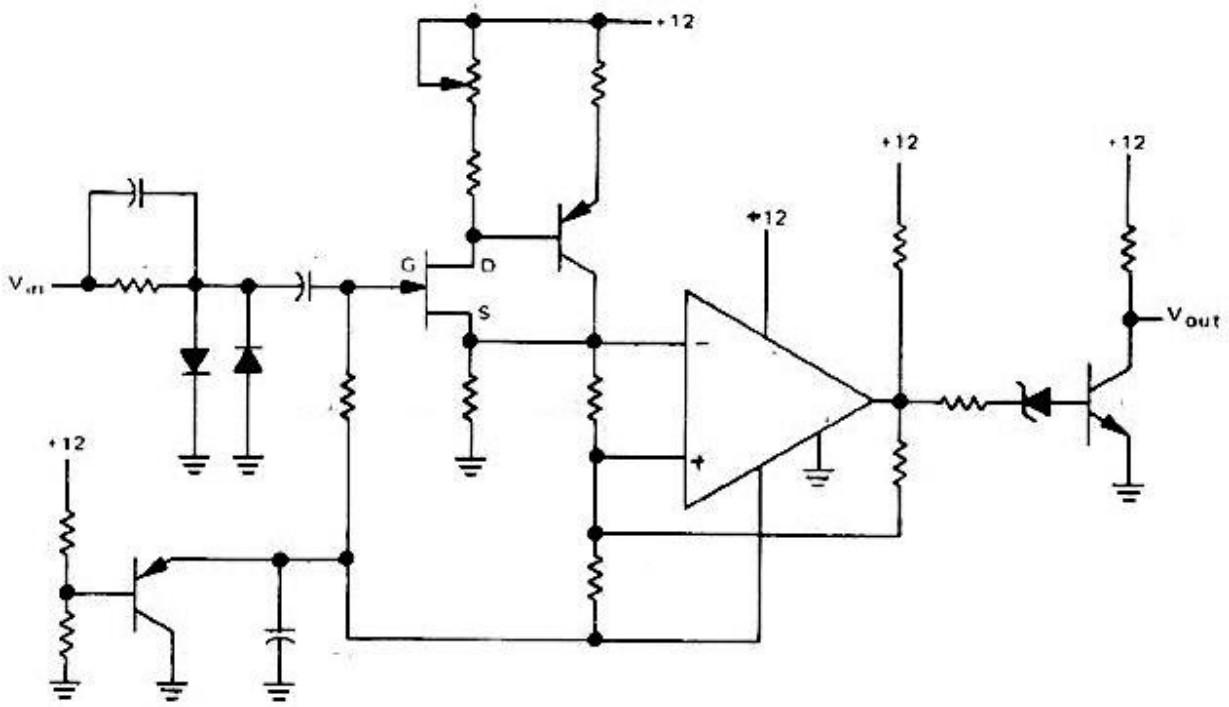
New England Radio
Discussion Society

May 2017 – AI2Q

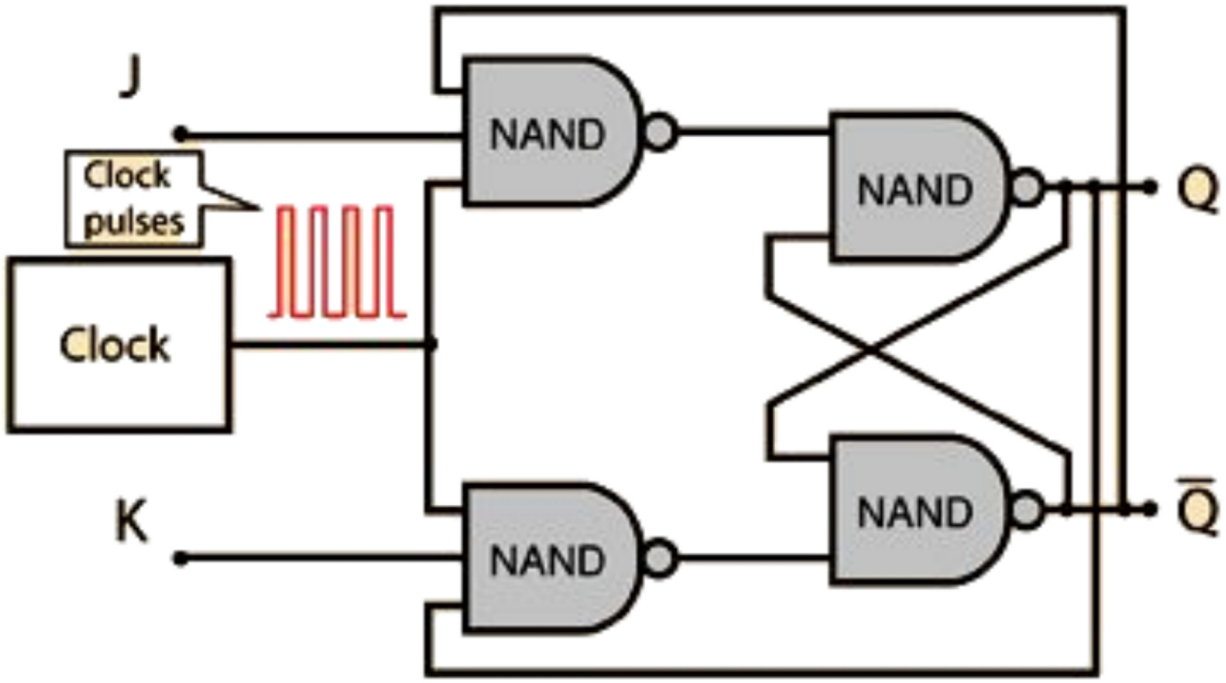
A circuit called a Schmitt trigger comparator readies analog signals for digital processing



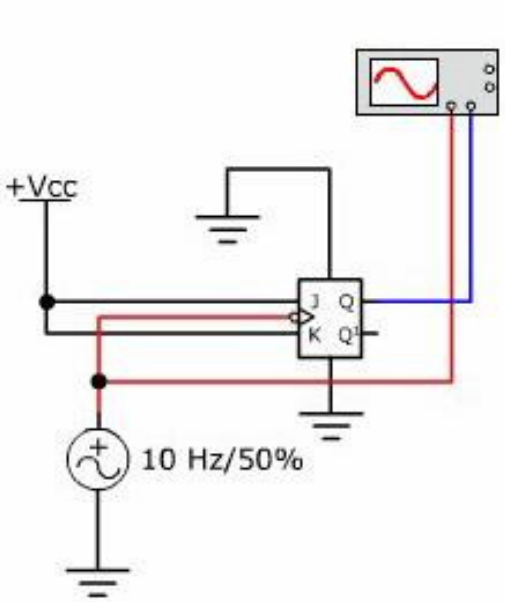
Here's a typical analog "front-end" for a frequency counter

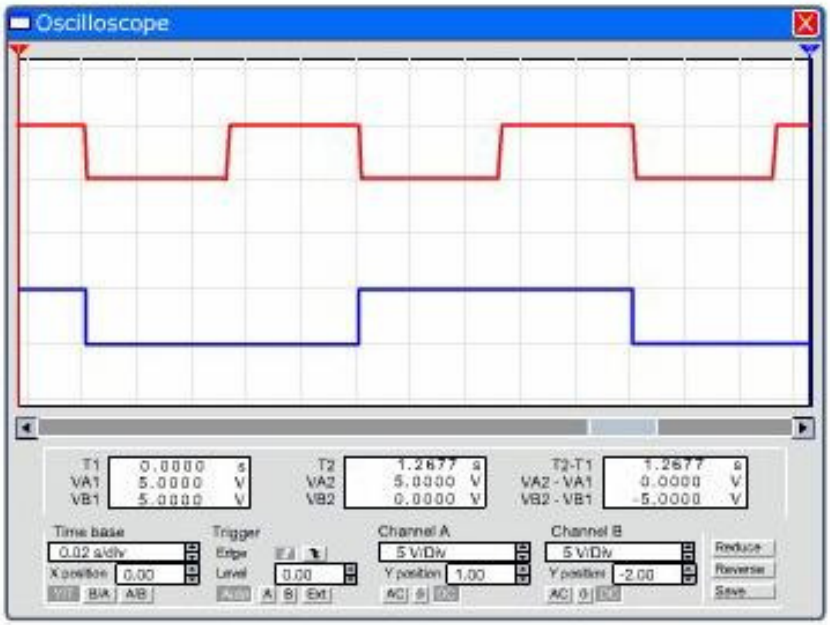


The *clocked* JK flip-flop forms the basis of circuits called *counters*

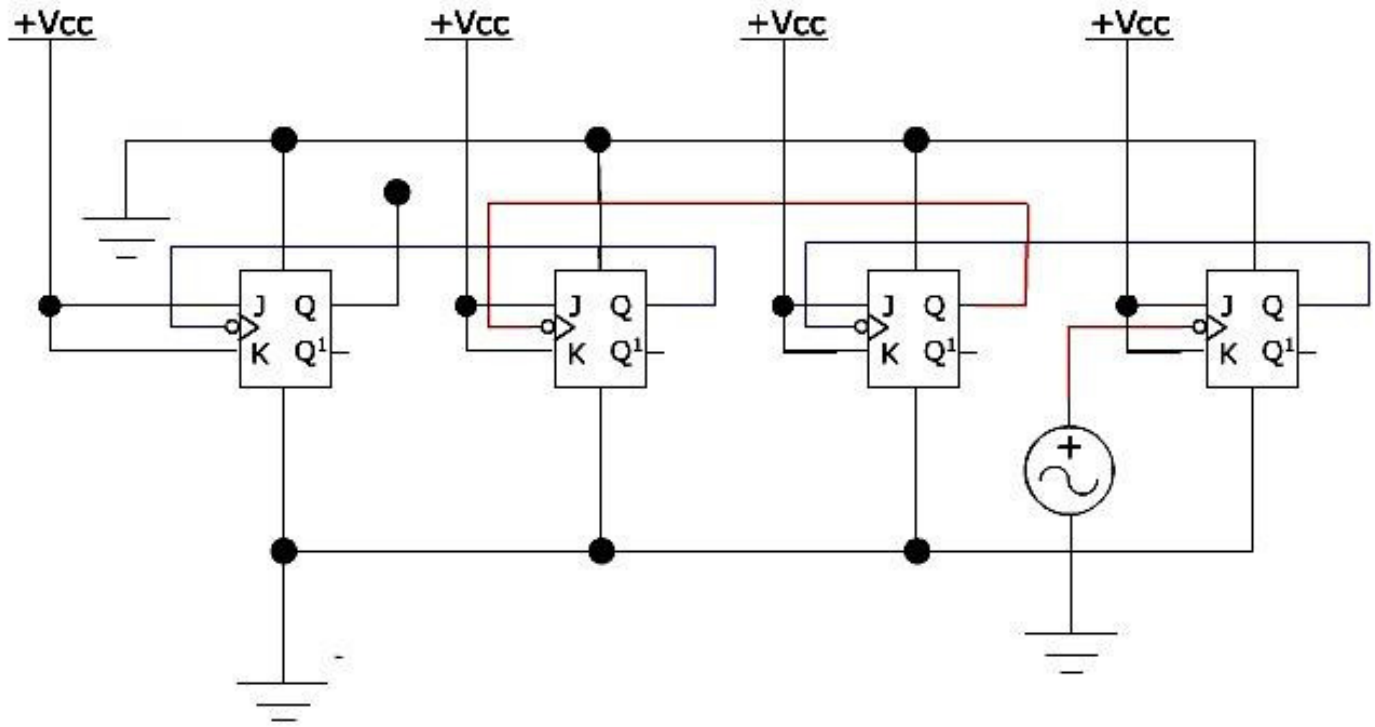


The JK flip-flop acts as a divider

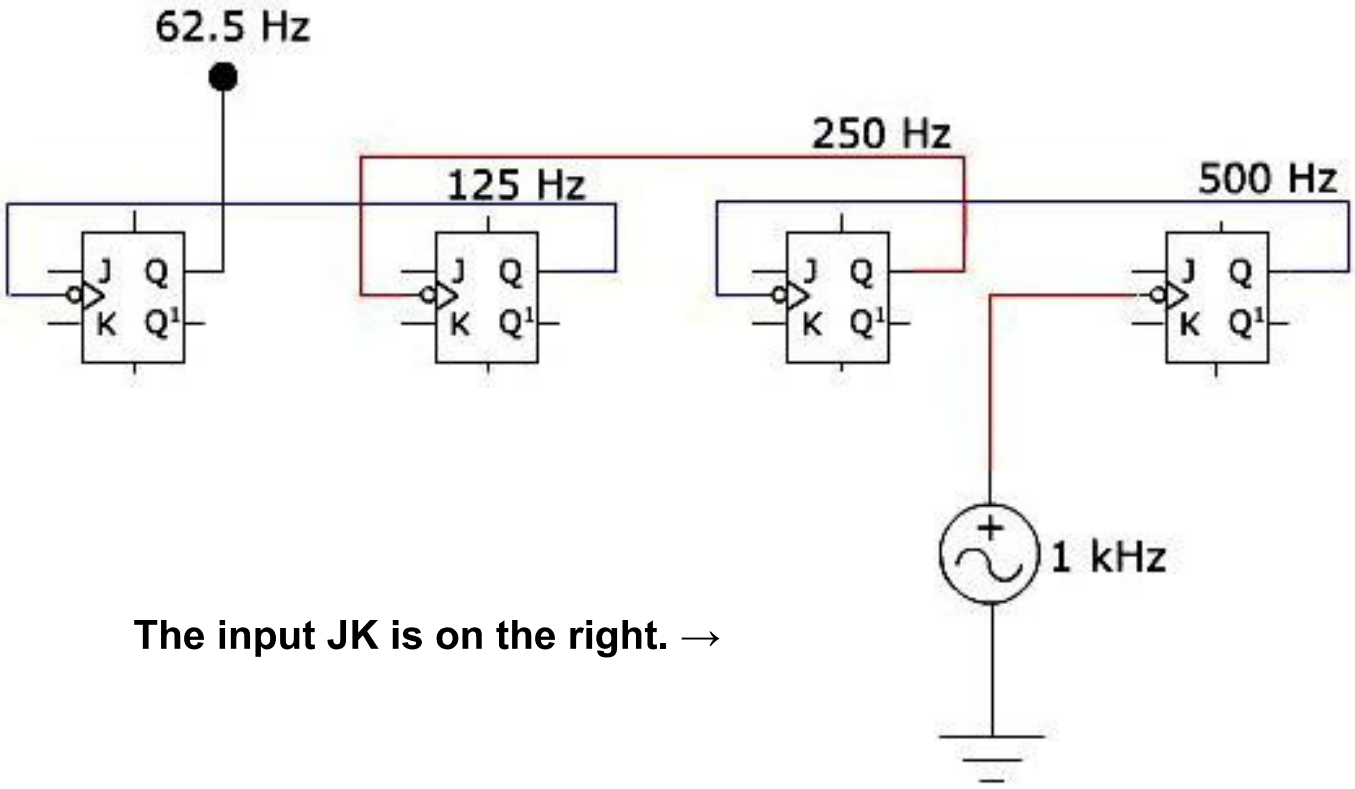




One JK flip-flop can feed another JK flip-flop



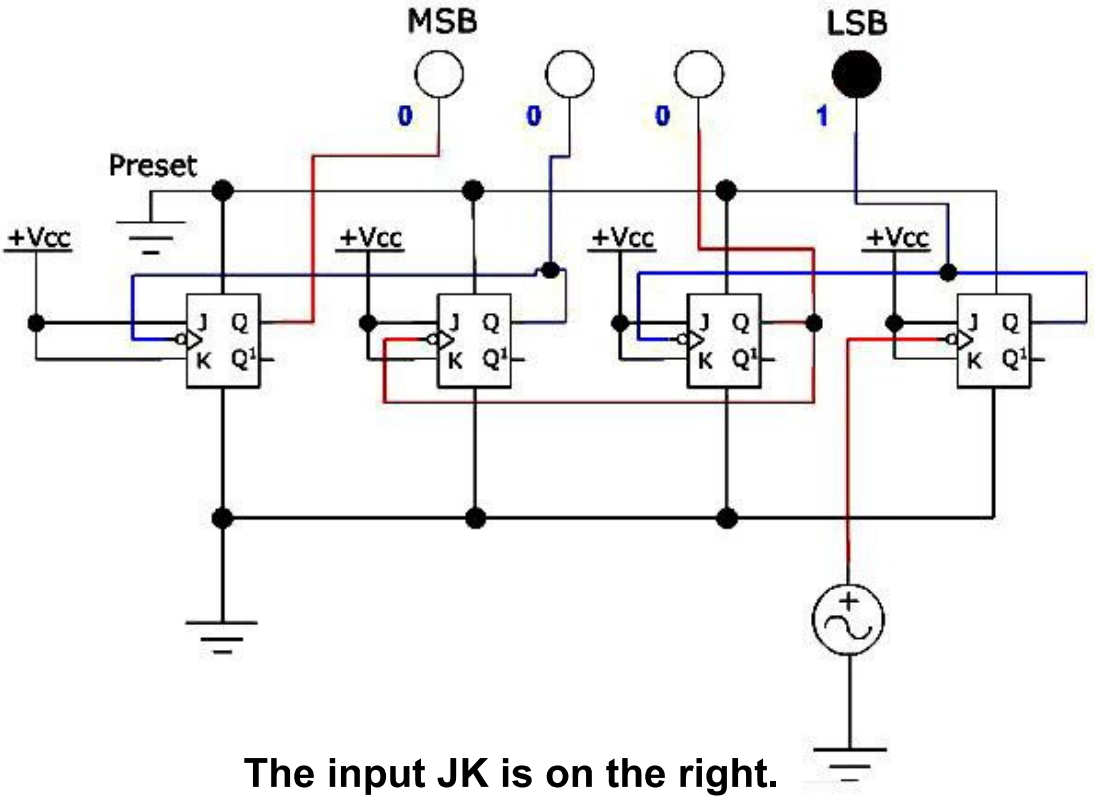
The output of one flip-flop can be used to "clock" the next stage. With each stage, the frequency is divided in half.



The input JK is on the right. →

The first count

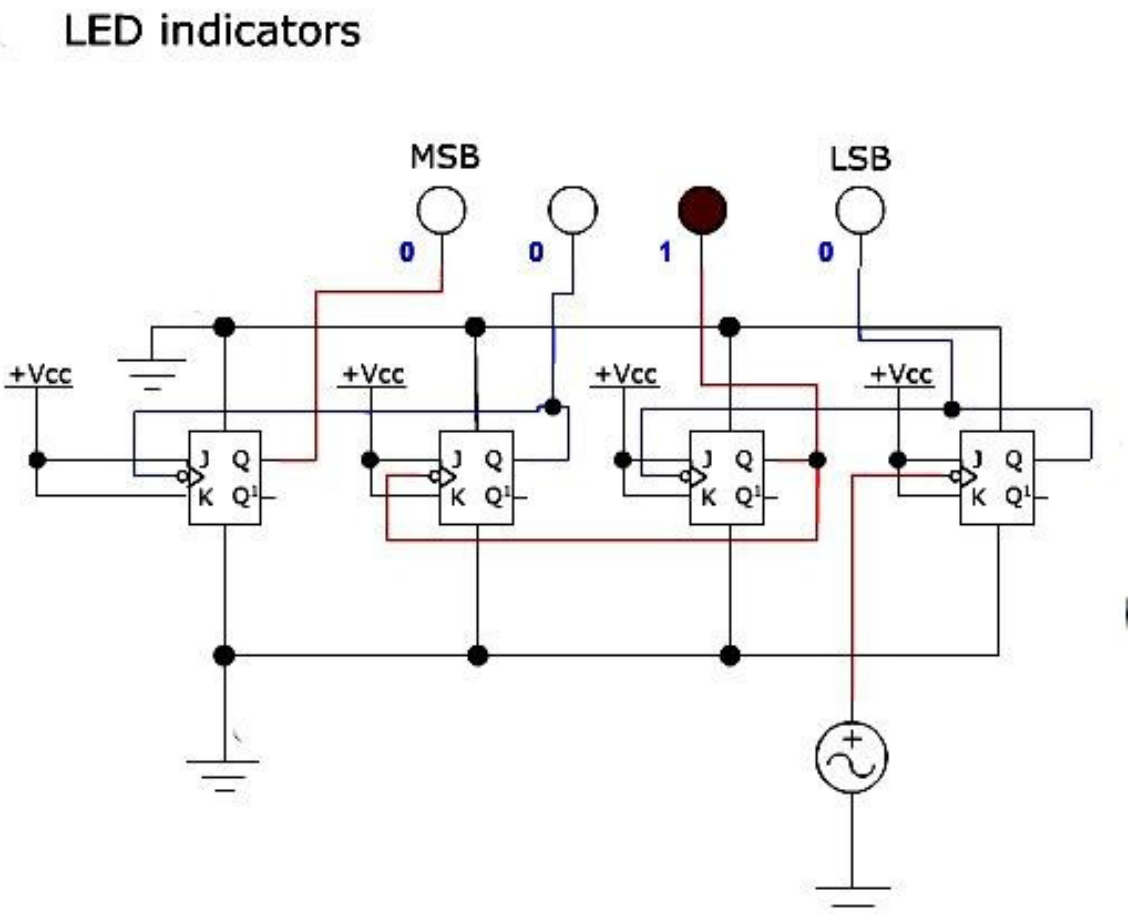
A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



The input JK is on the right.

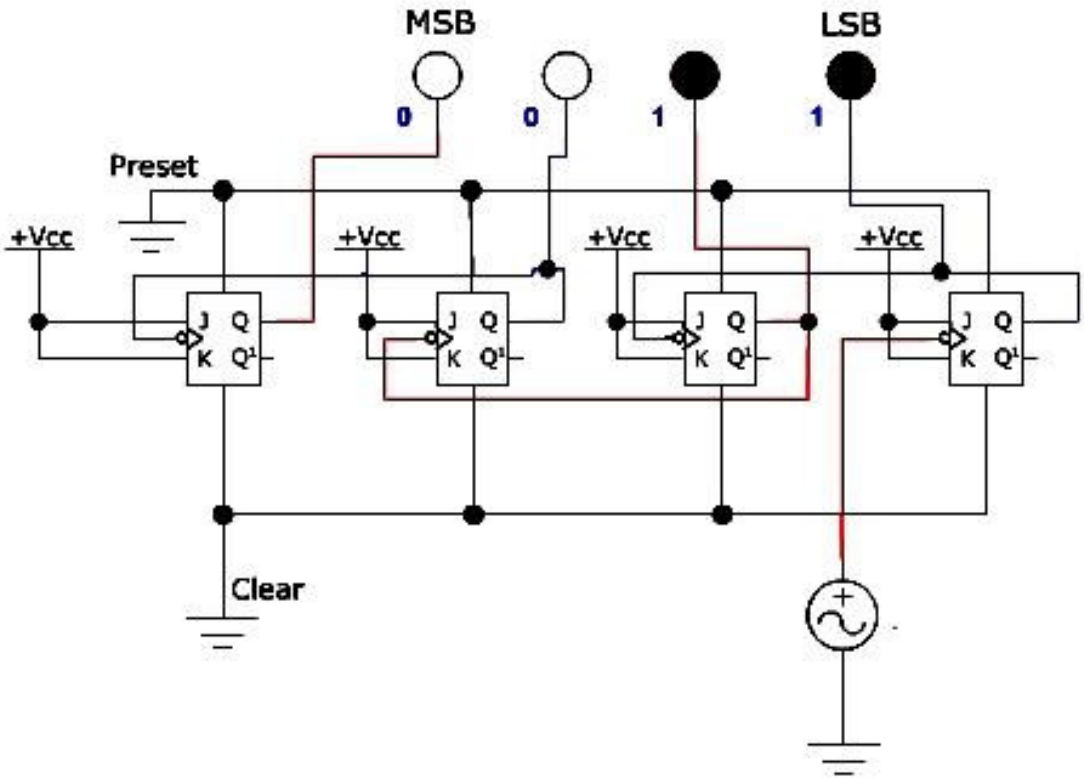
The next count is a binary 2

16 binary combinations	4 Inputs A	B	C	D
	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1



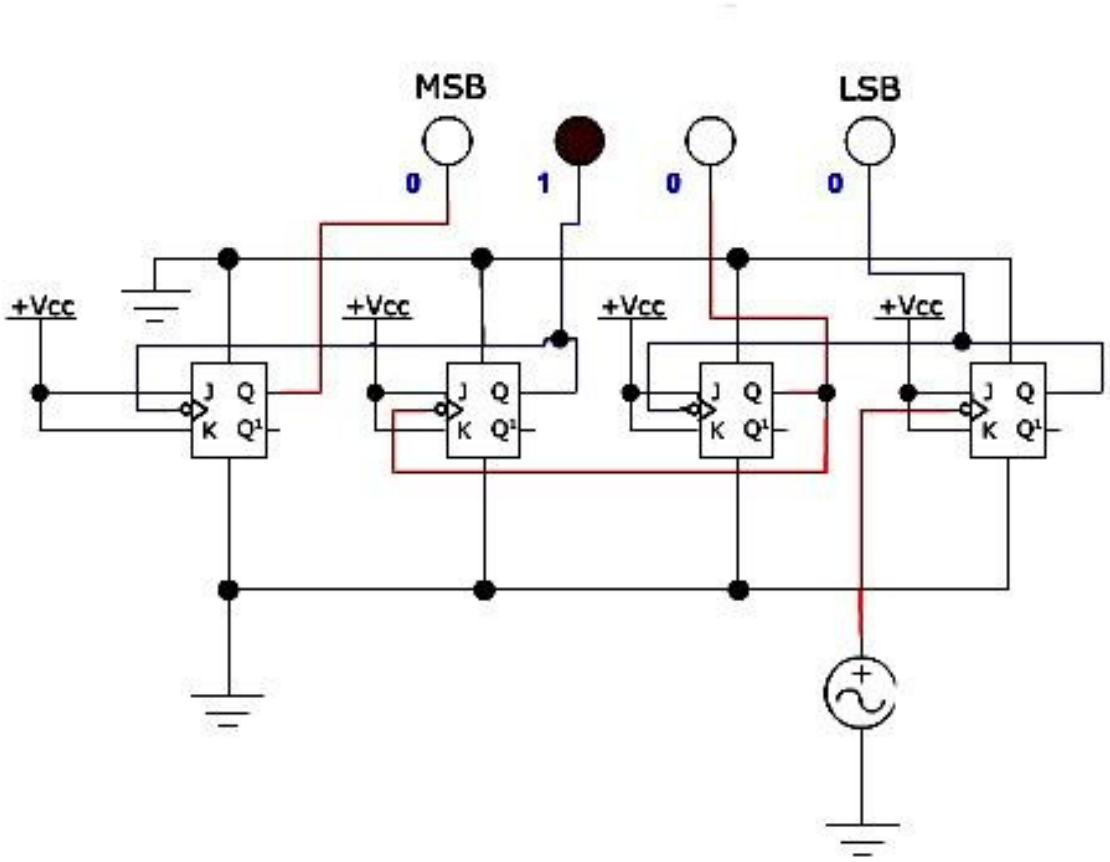
The count advances to a binary 3

16 binary combinations	4 Inputs A	B	C	D
	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1



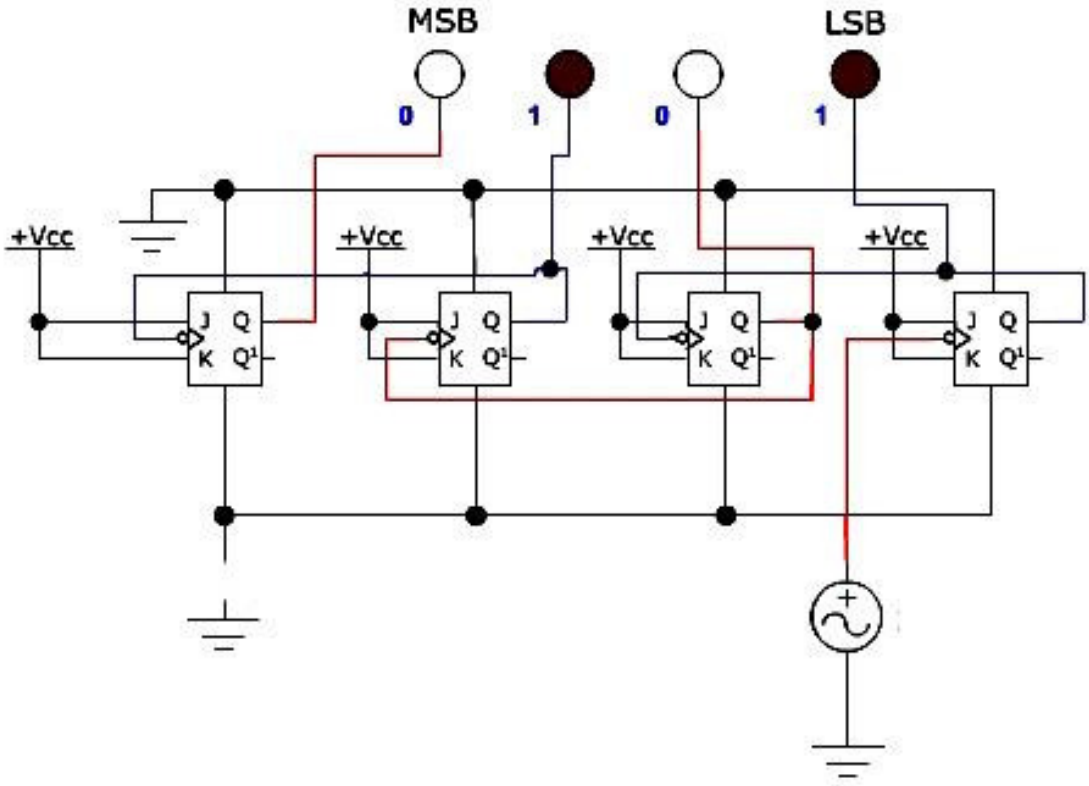
The count goes to a binary 4

4 Inputs				
	A	B	C	D
16 binary combinations	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1



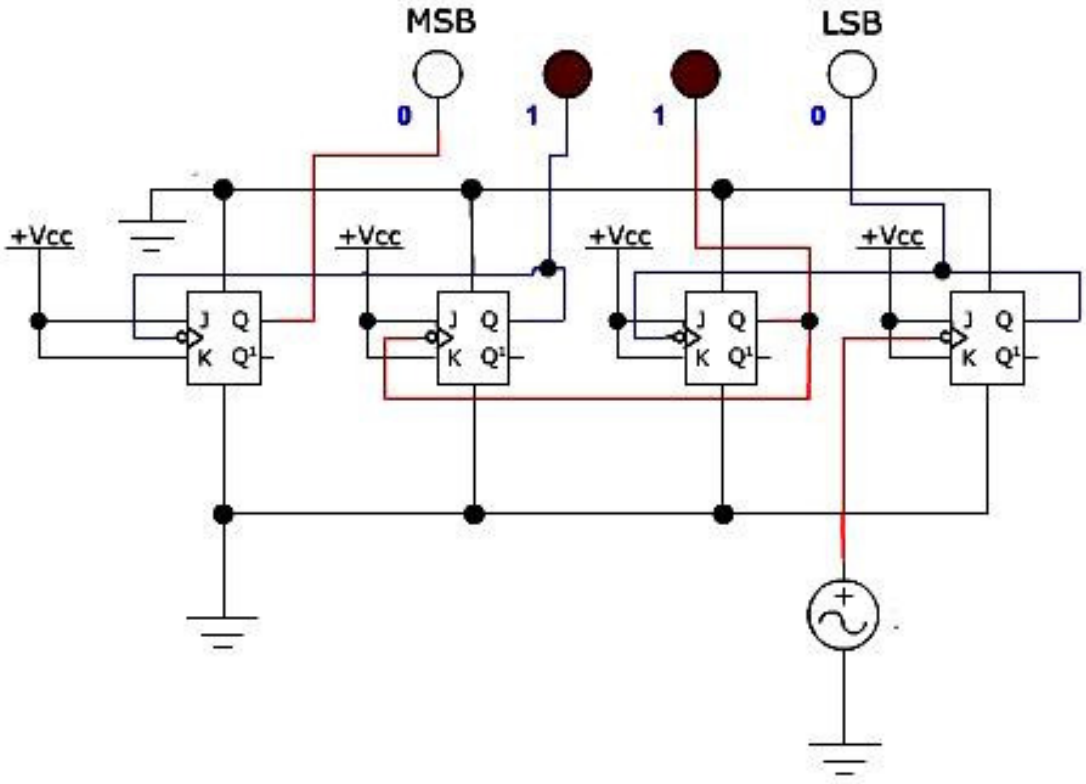
... then a binary 5

16 binary combinations	4 Inputs A	B	C	D
	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1



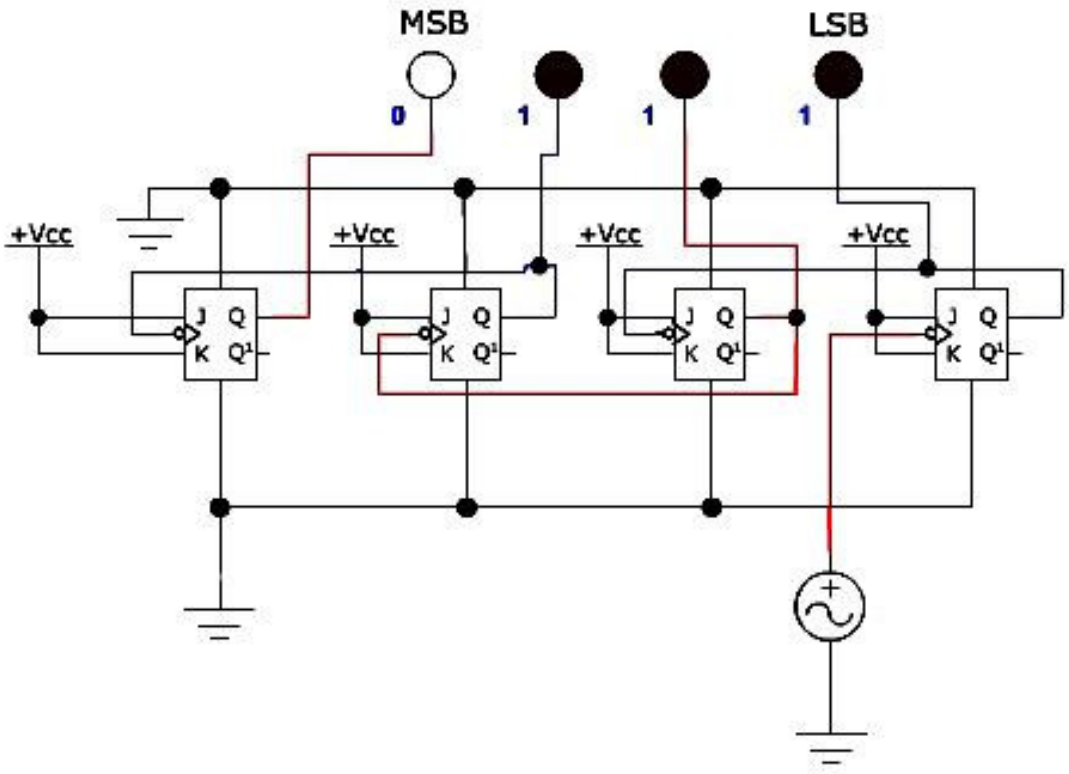
The count of 6

4 Inputs				
	A	B	C	D
16 binary combinations	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1



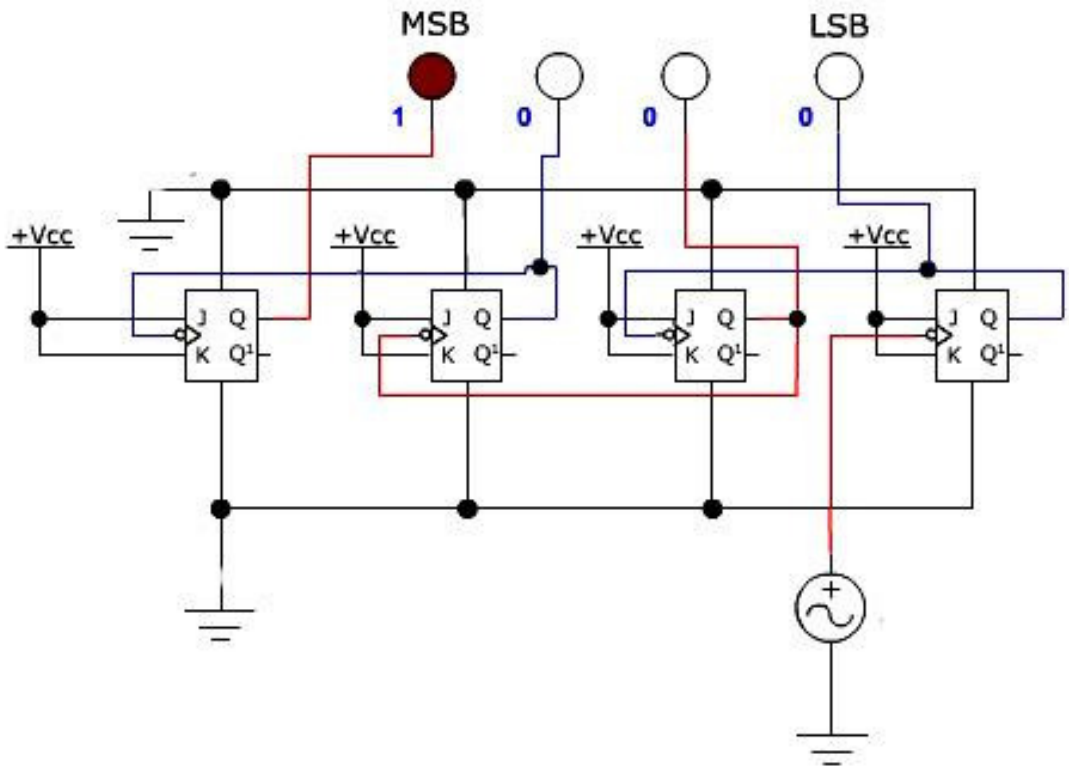
The count advances to a binary 7

4 Inputs				
	A	B	C	D
16 binary combinations	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1



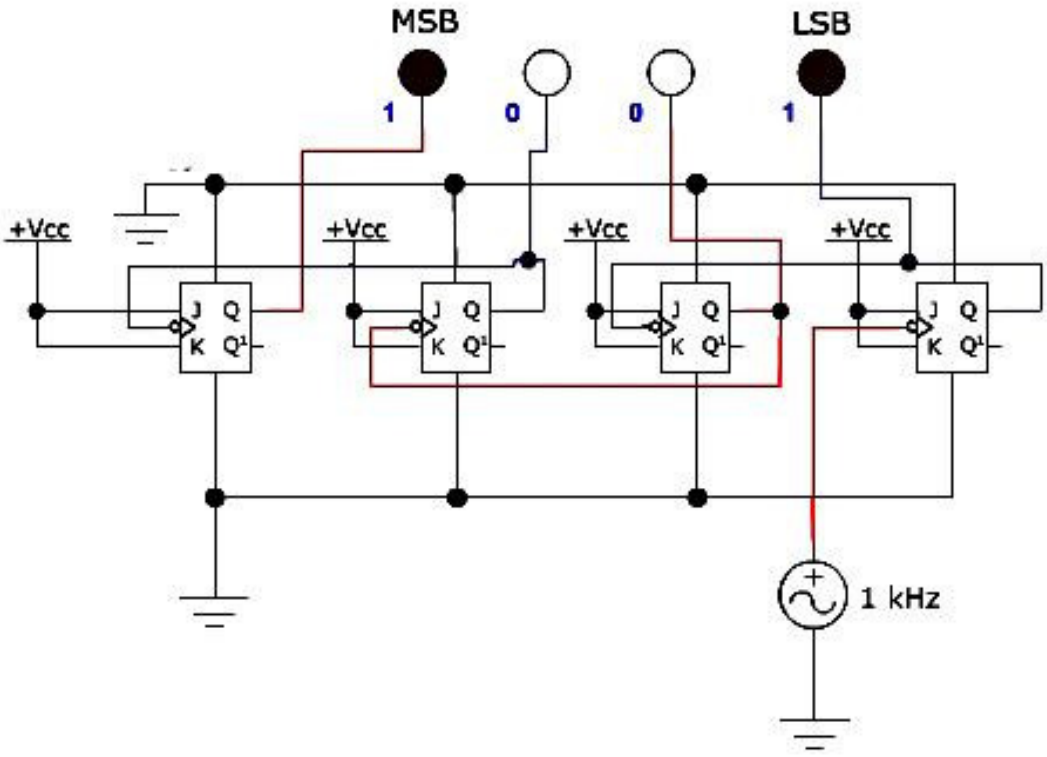
The count advances to 8

4 Inputs				
	A	B	C	D
16 binary combinations	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1

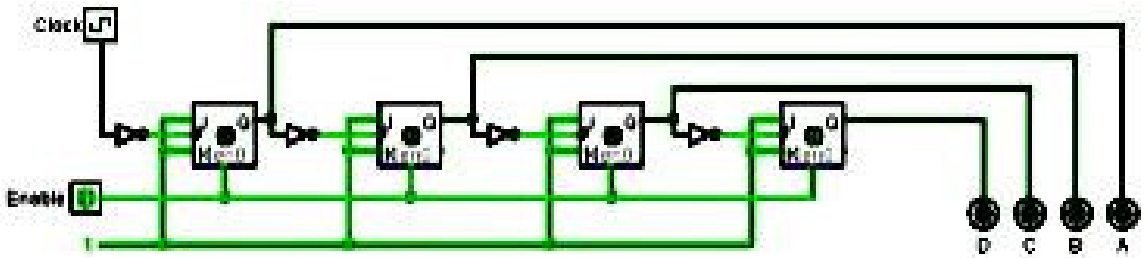


“Dressed to the nines”

4 Inputs				
	A	B	C	D
16 binary combinations	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1

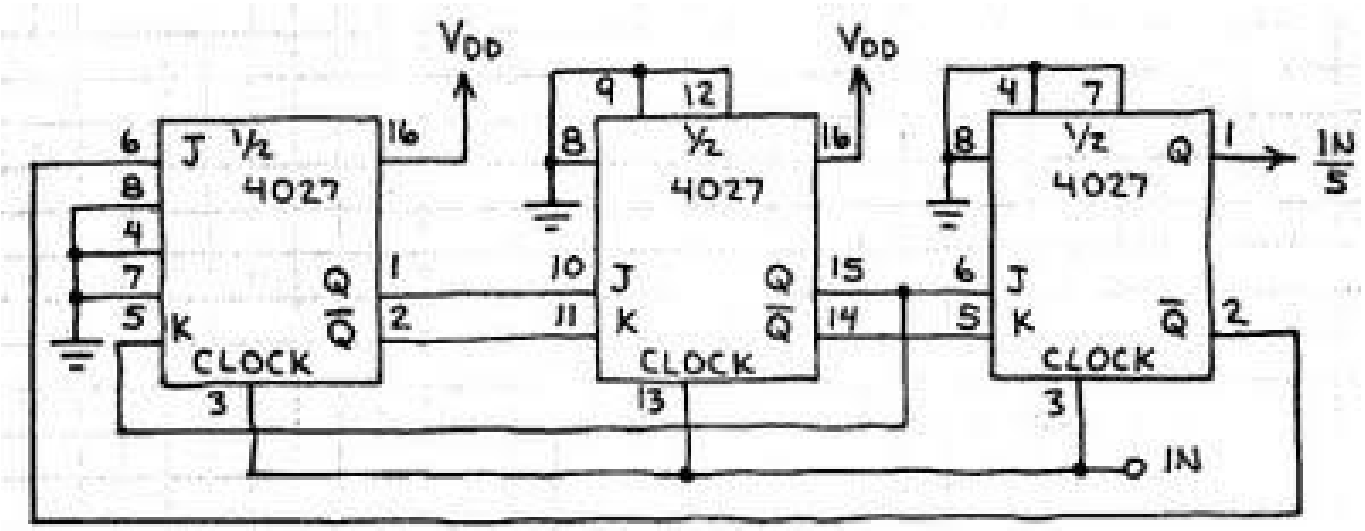


A 4-bit counter is called a *modulo 16* counter



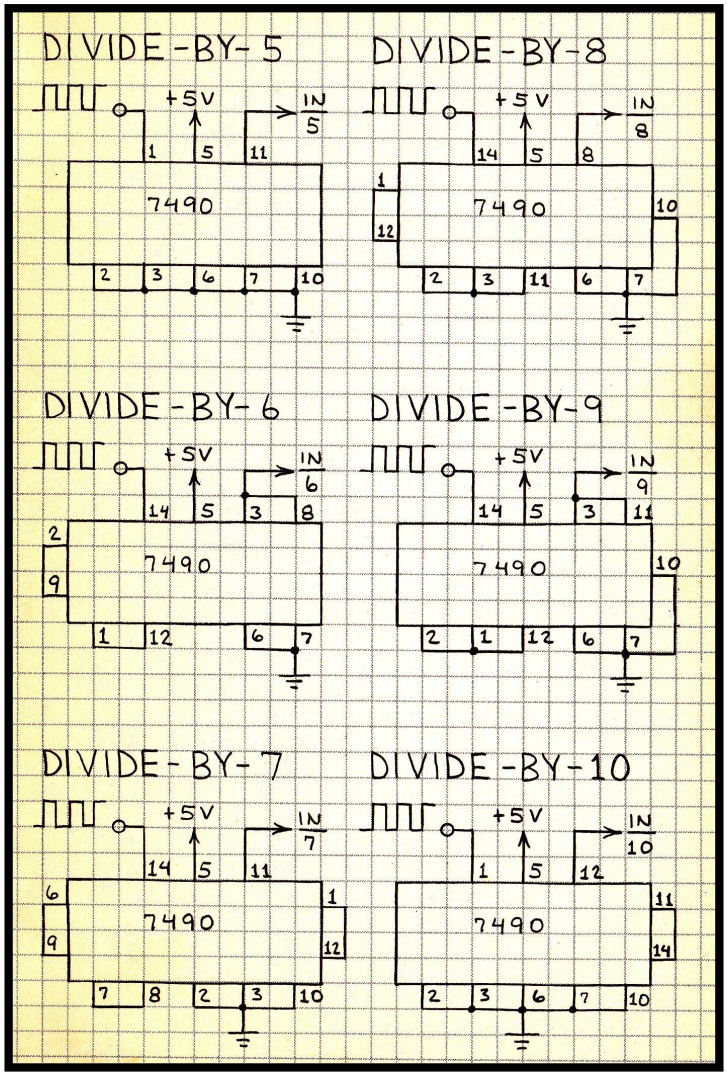
As the clock signal runs, the circuit will cycle its outputs through the values
0000, 0001, 0010, . . . , 1111
and then repeat the pattern.
So, it counts clock ticks, modulo 16.

Here's a divide-by-5 counter based on a 4000-Series 4027 CMOS chip



Here are some examples of TTL counter configurations based on 7490 *decade counter* chips

(*from Forrest Mims*)



BCD accommodates large numbers

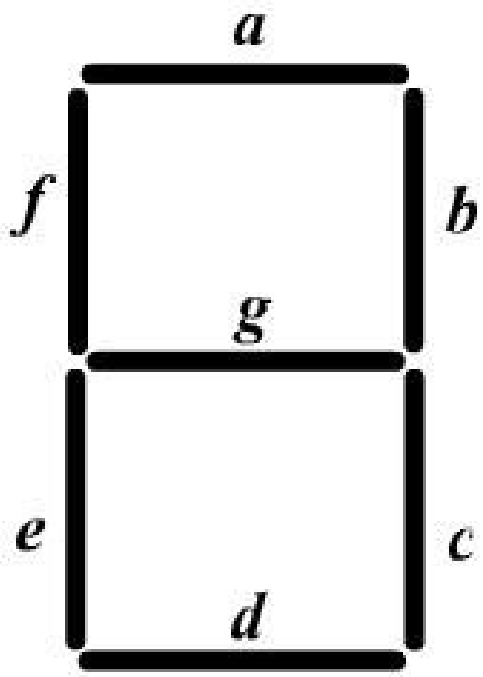
4	2	9
↓	↓	↓
0100	0010	1001

BCD code, 0100 0010 1001 is equivalent to 429.

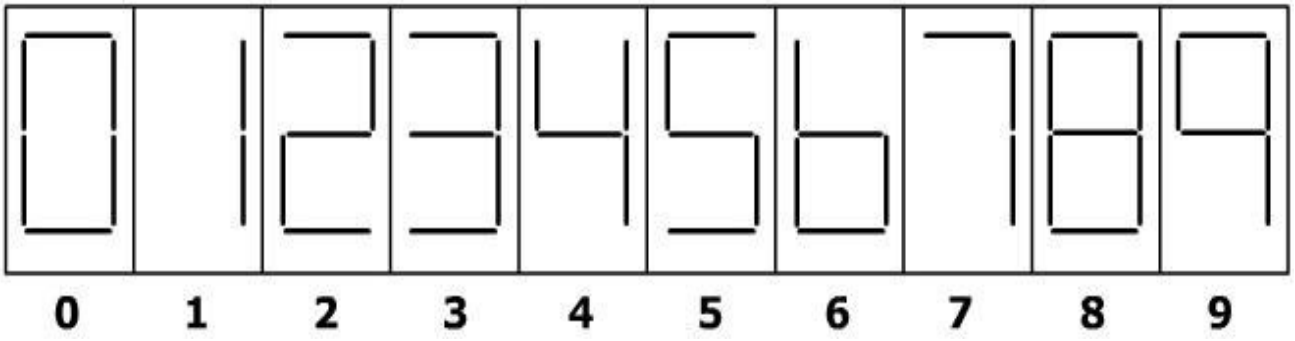
As another example, here is how to convert the decimal number 8963 to its BCD form:

8	9	6	3
↓	↓	↓	↓
1000	1001	0110	0011

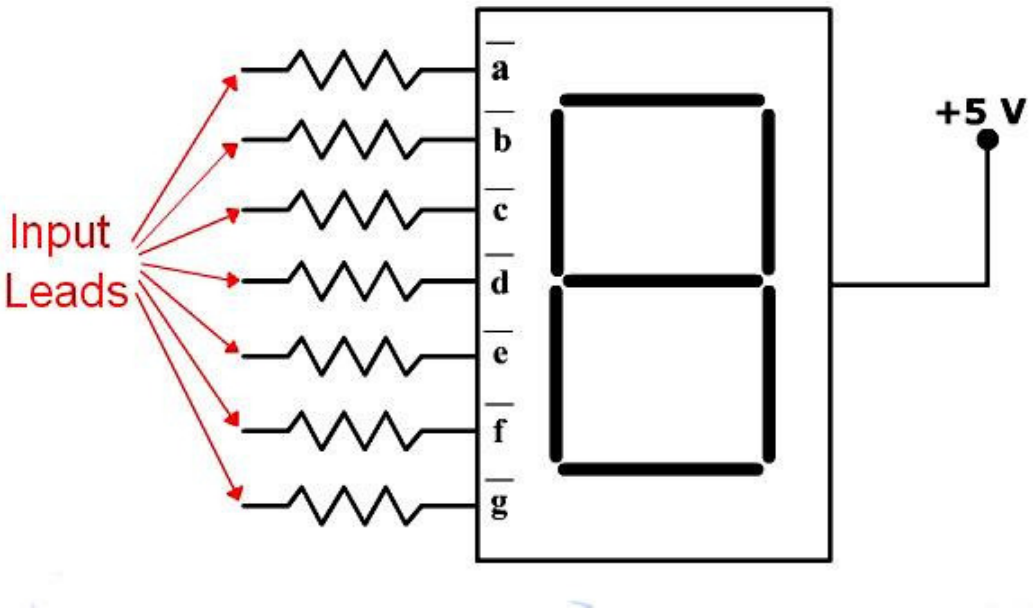
The common 7-segment display



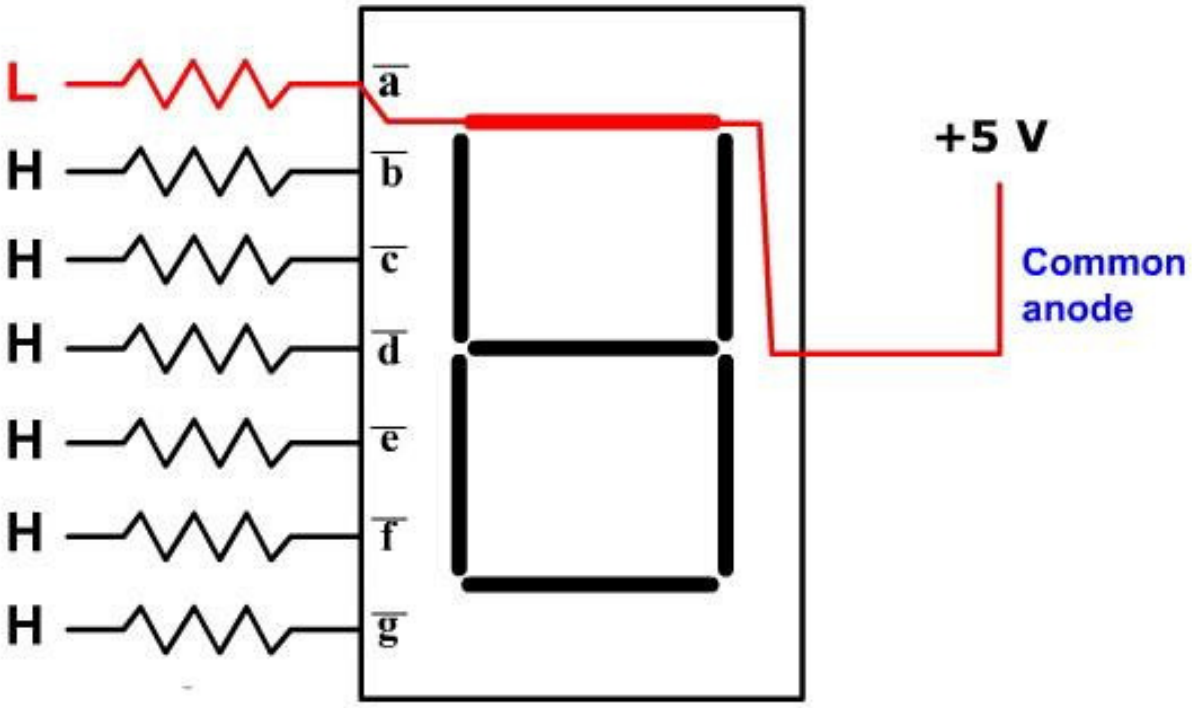
7-segment numbers



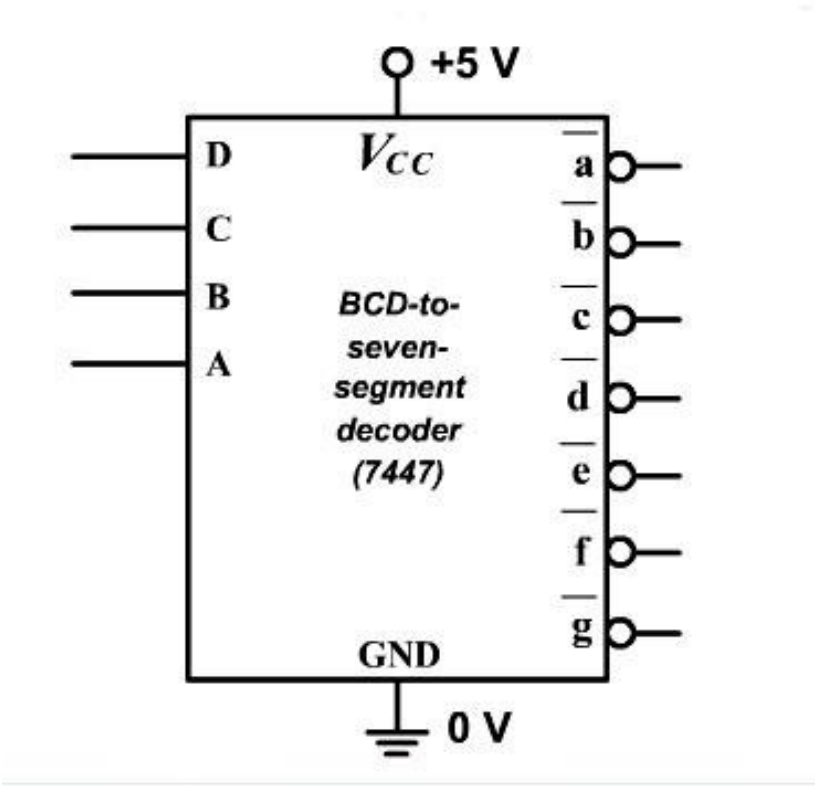
7-segment inputs



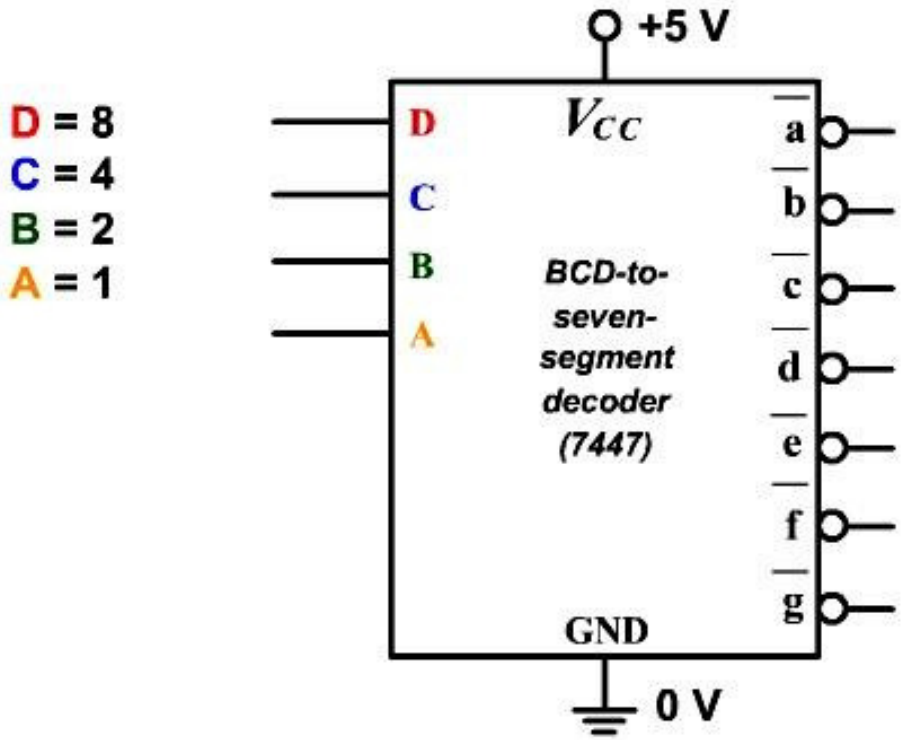
Driving a segment



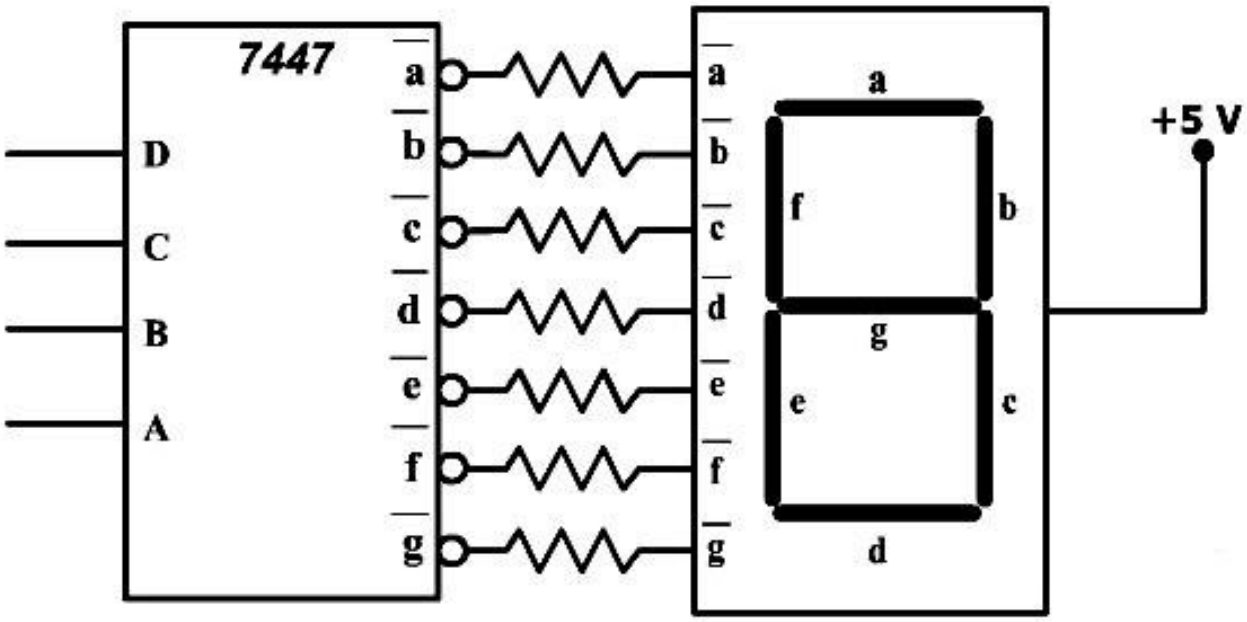
A TTL 7447 chip handles BCD to 7-segment conversion



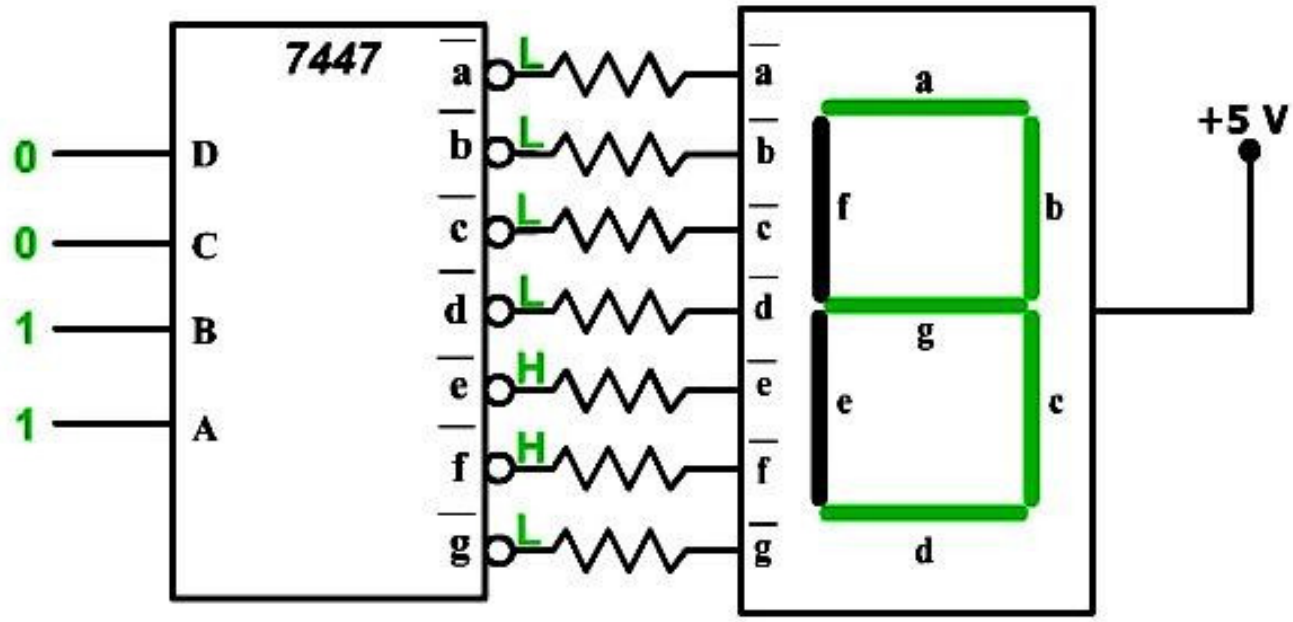
The 7447 IC has four input leads to which the 4-bit BCD numbers are applied. Each input is labeled with a capital letter, which represents one of the binary-weighted positional values.



7447 chip BCD connections



A 3-count decode



What to look for …….

The *reference oscillator* or *timebase*

- Aging and long-term stability
- Drift
- Short-term stability and jitter
- Adjustable to WWV?
- External reference inputs?

The *frequency tolerance* of a crystal or oscillator is defined as the initial deviation of the crystal or oscillator frequency as compared to the absolute value measured at 25°C.

The *frequency stability* over temp is defined as the frequency deviation compared to the measured frequency at 25°C OVER the defined operating temperature range (I.e. 0°C to +70°C).

Stability tolerance is sometimes expressed as a percentage of frequency deviation rather than as *parts per million* (PPM).

For example:

0.01 % = 100 PPM
0.005% = 50 PPM
0.001 % = 10 PPM

etc.

The stability tolerance of a crystal or oscillator needs to be specified, along with the operating temperature range.

For example, a xtal may be specified as having a frequency stability tolerance of ±50 PPM over an operating temperature of -45°C to + 85°C, and having a frequency tolerance of ±50 PPM at +25°C.

Gating

Ideally, a precisely timed gate-enabling clock signal is applied to one input of a F-F gate. The other gate accepts conditioned pulses from the incoming signal.

The output is a series of pulses for a precise amount of time.

For example, if the incoming signal is 1-MHz and the gate was opened for 1 second, then 1 million pulses would clock through.

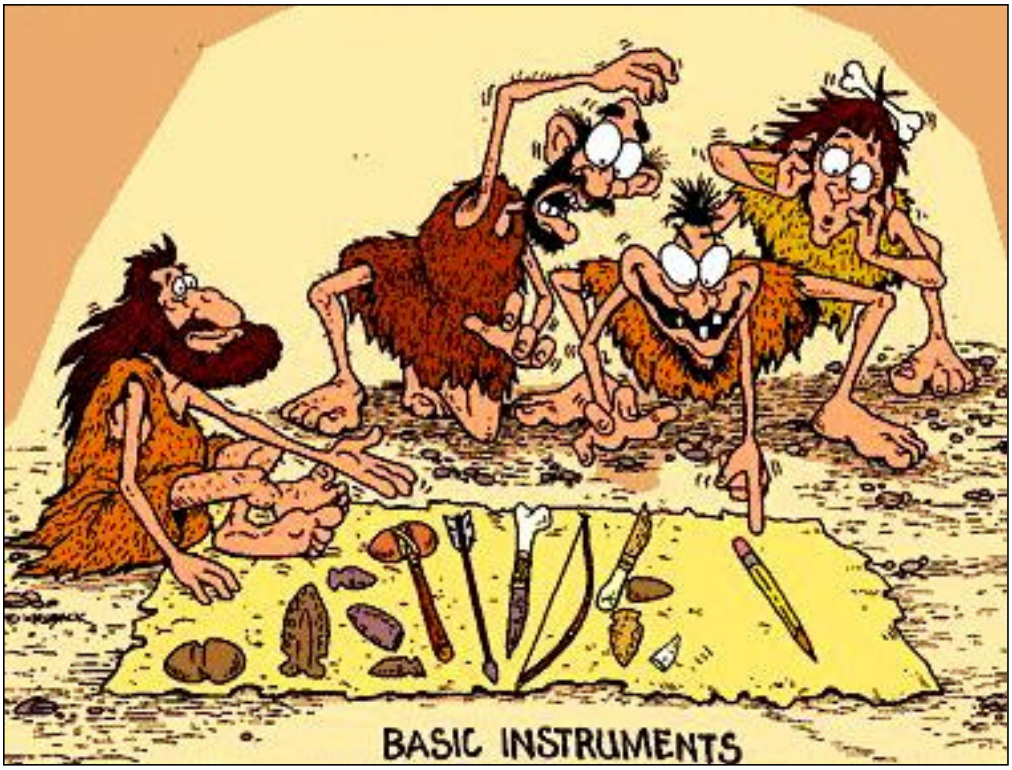
Shorter gate times enable displays to be refreshed more often, but count accuracy is reduced.

For example, a gate time of 1-second will enable frequency resolution of 1 Hz, but a 10-sec gate time enables resolution down to 0.1 Hz.

Counter functions and features

- Readability
- Resolution
- Other functions and on-screen indications
- Portability
- Period counting
- Input overload protection
- Trigger point adjustability
- Input impedance
- Variable gating

That’s the basics of our friend the frequency counter!



That’s all for now!
73 DE AI2Q